



TGF2023-2-20

100 W, 32 V, DC to 14 GHz, Discrete Power GaN on SiC HEMT

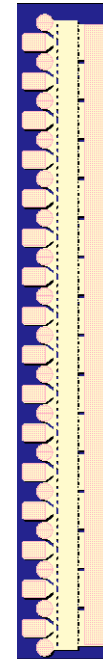
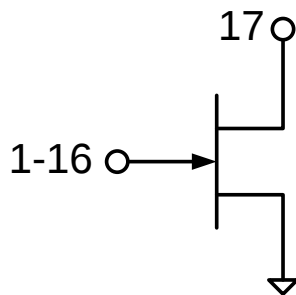
Product Overview

The Qorvo TGF2023-2-20 is a discrete 20 mm GaN on SiC HEMT which operates from DC-14 GHz. The TGF2023-2-20 is designed using Qorvo's proven QGaN25 production process. This process features advanced field plate techniques to optimize microwave power and efficiency at high drain bias operating conditions.

The TGF2023-2-20 typically provides 50.2 dBm of saturated output power with power gain of 14 dB at 6 GHz. The maximum power added efficiency is 65.1% which makes the TGF2023-2-20 appropriate for high efficiency applications.

Lead-free and RoHS compliant

Functional Block Diagram



Key Features

- Frequency Range: DC - 14 GHz
 - Output Power (P_{3dB})¹: 50.2 dBm
 - Maximum PAE¹: 65.1%
 - Linear Gain¹: 17 dB
 - Bias: $V_D = 12 - 32$ V, $I_{DQ} = 400 - 2000$ mA
 - Technology: QGaN25 on SiC
 - Chip Dimensions: 0.82 x 4.56 x 0.10 mm
- Note 1: @ 6 GHz

Applications

- Defense & Aerospace
- Broadband Wireless

Pad Configuration

Pad No.	Symbol
1-16	V_G / RF IN
17	V_D / RF OUT
Backside	Source / Ground

Ordering Information

Part Number	Description
TGF2023-2-20	100 Watt GaN HEMT

Absolute Maximum Ratings

Parameter	Rating
Drain to Gate Voltage (V_{DG})	100 V
Gate Voltage Range (V_G)	-7 to +2 V
Drain Current (I_D)	20 A
Gate Current (I_G)	-20 to 56 mA
Power Dissipation, CW (P_D)	See graph on pg.4.
CW Input Power (P_{IN})	+43 dBm
Storage Temperature	-65 to 150°C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Drain Voltage Range (V_D)	–	+28	–	V
Drain Quiescent Current (I_{DQ})	–	1000	–	mA
Gate Voltage, V_G ¹	-3.7	-2.8	-2.3	V
Gate Leakage: $V_D = +10$ V, $V_G = -3.7$ V	-20	–	–	mA

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Note:

1. To be adjusted to desired I_{DQ}

RF Characterization – Model Optimum Power Tune

Test conditions unless otherwise noted: T = 25°C, Pulse (10% Duty Cycle, 100 μ s Width).

Parameter	Typical Value								Units
Frequency (F)	3		6		8		10		GHz
Drain Voltage (V_D)	28	28	28	28	28	28	28	28	V
Bias Current (I_{DQ})	400	1000	400	1000	400	1000	400	1000	mA
Output P3dB (P_{3dB})	50.3	50.2	50.2	50.2	50.2	50.1	50.2	50.2	dBm
PAE @ P_{3dB} (PAE_{3dB})	62.4	61.7	58.7	58.6	56.1	56	53	53.3	%
Gain @ P_{3dB} (G_{3dB})	19.1	19.9	13.2	14	10.7	11.5	9.0	9.6	dB
Parallel Resistance ⁽¹⁾ (R_p)	64.4	64.8	59.7	59.2	54.8	54.4	49.6	49.2	Ω ·mm
Parallel Capacitance ⁽¹⁾ (C_p)	0.264	0.255	0.291	0.295	0.317	0.315	0.326	0.324	pF/mm
Load Reflection Coefficient ⁽²⁾ (Γ_L)	0.20 $\angle$ 131°	0.20 $\angle$ 131°	0.38 $\angle$ 132°	0.38 $\angle$ 132°	0.49 $\angle$ 137°	0.49 $\angle$ 138°	0.57 $\angle$ 143°	0.56 $\angle$ 143°	--

Notes:

1. Large signal equivalent output network (normalized).
2. Characteristic Impedance (Z_0) = 4 Ω .

RF Characterization – Model Optimum Efficiency Tune

Test conditions unless otherwise noted: T = 25°C, Pulse (10% Duty Cycle, 100 μ s Width).

Parameter	Typical Value								Units
Frequency (F)	3		6		8		10		GHz
Drain Voltage (V_D)	28	28	28	28	28	28	28	28	V
Bias Current (I_{DQ})	400	1000	400	1000	400	1000	400	1000	mA
Output P3dB (P_{3dB})	48.5	48.7	48.8	48.9	49.0	49.1	49.2	49.1	dBm
PAE @ P_{3dB} (PAE_{3dB})	69.5	68.5	66	65.1	62.2	61.8	58.4	58.4	%
Gain @ P_{3dB} (G_{3dB})	21.1	21.7	14.7	15.2	11.8	12.5	10.1	10.6	dB
Parallel Resistance ⁽¹⁾ (R_p)	126	123	110	103	94.9	90.3	81.6	80.5	Ω ·mm
Parallel Capacitance ⁽¹⁾ (C_p)	0.392	0.385	0.388	0.387	0.379	0.379	0.373	0.378	pF/mm
Load Reflection Coefficient ⁽²⁾ (Γ_L)	0.40 $\angle$ 78°	0.39 $\angle$ 78°	0.58 $\angle$ 111°	0.56 $\angle$ 112°	0.64 $\angle$ 124°	0.63 $\angle$ 125°	0.69 $\angle$ 133°	0.69 $\angle$ 133°	--

Notes:

1. Large signal equivalent output network (normalized).
2. Characteristic Impedance (Z_0) = 4 Ω .

Thermal and Reliability Information - CW ⁽¹⁾

Parameter	Test Conditions	Value	Units
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	$P_{DISS} = 20\text{ W}$, $T_{baseplate} = 85^{\circ}\text{C}$	1.5	$^{\circ}\text{C/W}$
Channel Temperature, T_{CH}		114	$^{\circ}\text{C}$
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	$P_{DISS} = 30\text{ W}$, $T_{baseplate} = 85^{\circ}\text{C}$	1.6	$^{\circ}\text{C/W}$
Channel Temperature, T_{CH}		132	$^{\circ}\text{C}$
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	$P_{DISS} = 40\text{ W}$, $T_{baseplate} = 85^{\circ}\text{C}$	1.6	$^{\circ}\text{C/W}$
Channel Temperature, T_{CH}		149	$^{\circ}\text{C}$
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	$P_{DISS} = 50\text{ W}$, $T_{baseplate} = 85^{\circ}\text{C}$	1.6	$^{\circ}\text{C/W}$
Channel Temperature, T_{CH}		167	$^{\circ}\text{C}$
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	$P_{DISS} = 60\text{ W}$, $T_{baseplate} = 85^{\circ}\text{C}$	1.7	$^{\circ}\text{C/W}$
Channel Temperature, T_{CH}		187	$^{\circ}\text{C}$

Notes:

- Assumes eutectic attach using 1.5mil thick 80/20 AuSn mounted to a 10 mm x 10 mm x 40 mil CuMo Carrier Plate.
- Refer to the following document: [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates](#)

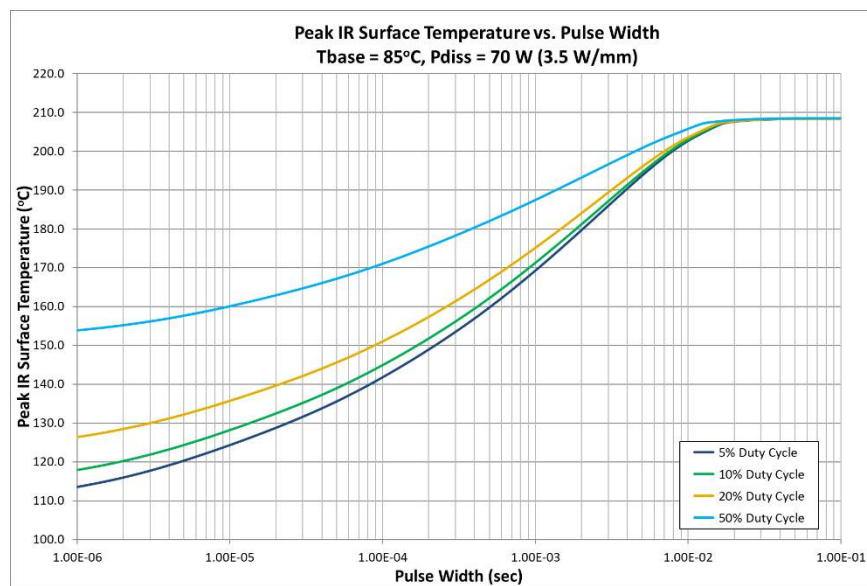
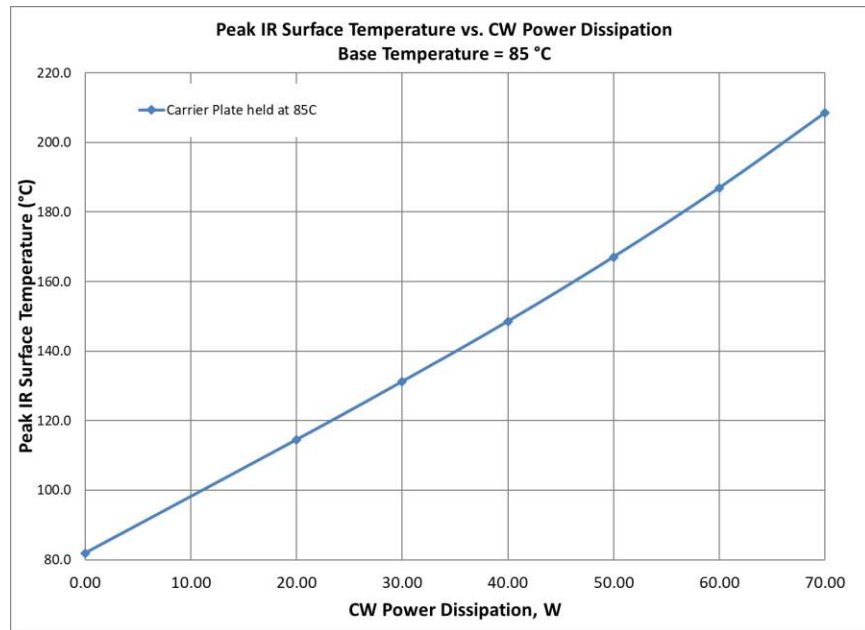
Thermal and Reliability Information - Pulsed ⁽¹⁾

Parameter	Test Conditions	Value	Units
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	$P_{DISS} = 70\text{ W}$, $T_{baseplate} = 85^{\circ}\text{C}$ Pulse Width = 100 μS	0.8	$^{\circ}\text{C/W}$
Channel Temperature, T_{CH}		142	$^{\circ}\text{C}$
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	$P_{DISS} = 70\text{ W}$, $T_{baseplate} = 85^{\circ}\text{C}$ Pulse Width = 100 μS	0.9	$^{\circ}\text{C/W}$
Channel Temperature, T_{CH}		145	$^{\circ}\text{C}$
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	$P_{DISS} = 70\text{ W}$, $T_{baseplate} = 85^{\circ}\text{C}$ Pulse Width = 100 μS	0.9	$^{\circ}\text{C/W}$
Channel Temperature, T_{CH}		151	$^{\circ}\text{C}$
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	$P_{DISS} = 70\text{ W}$, $T_{baseplate} = 85^{\circ}\text{C}$ Pulse Width = 100 μS	1.2	$^{\circ}\text{C/W}$
Channel Temperature, T_{CH}		171	$^{\circ}\text{C}$

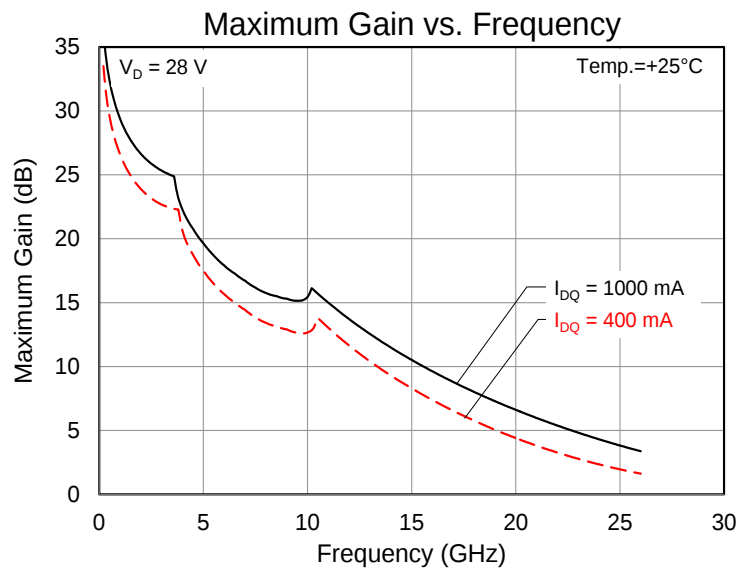
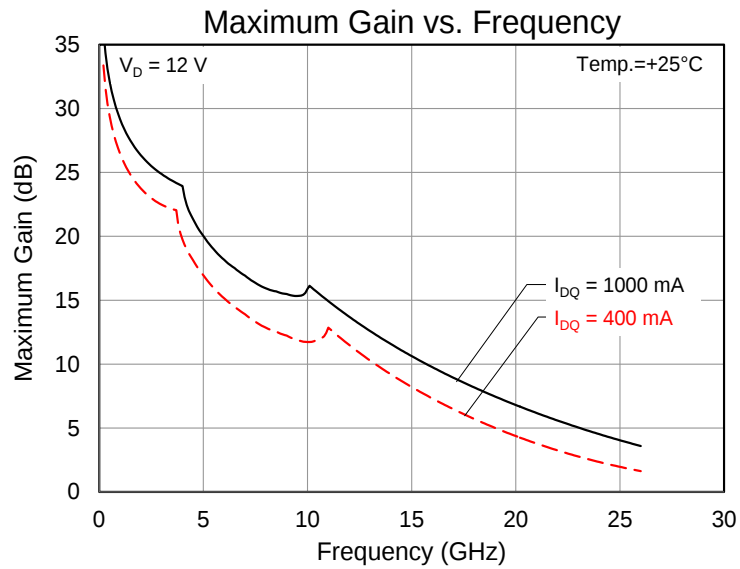
Notes:

- Assumes eutectic attach using 1.5mil thick 80/20 AuSn mounted to a 10 mm x 10 mm x 40 mil CuMo Carrier Plate.
- Refer to the following document: [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates](#)

Maximum Channel Temperature



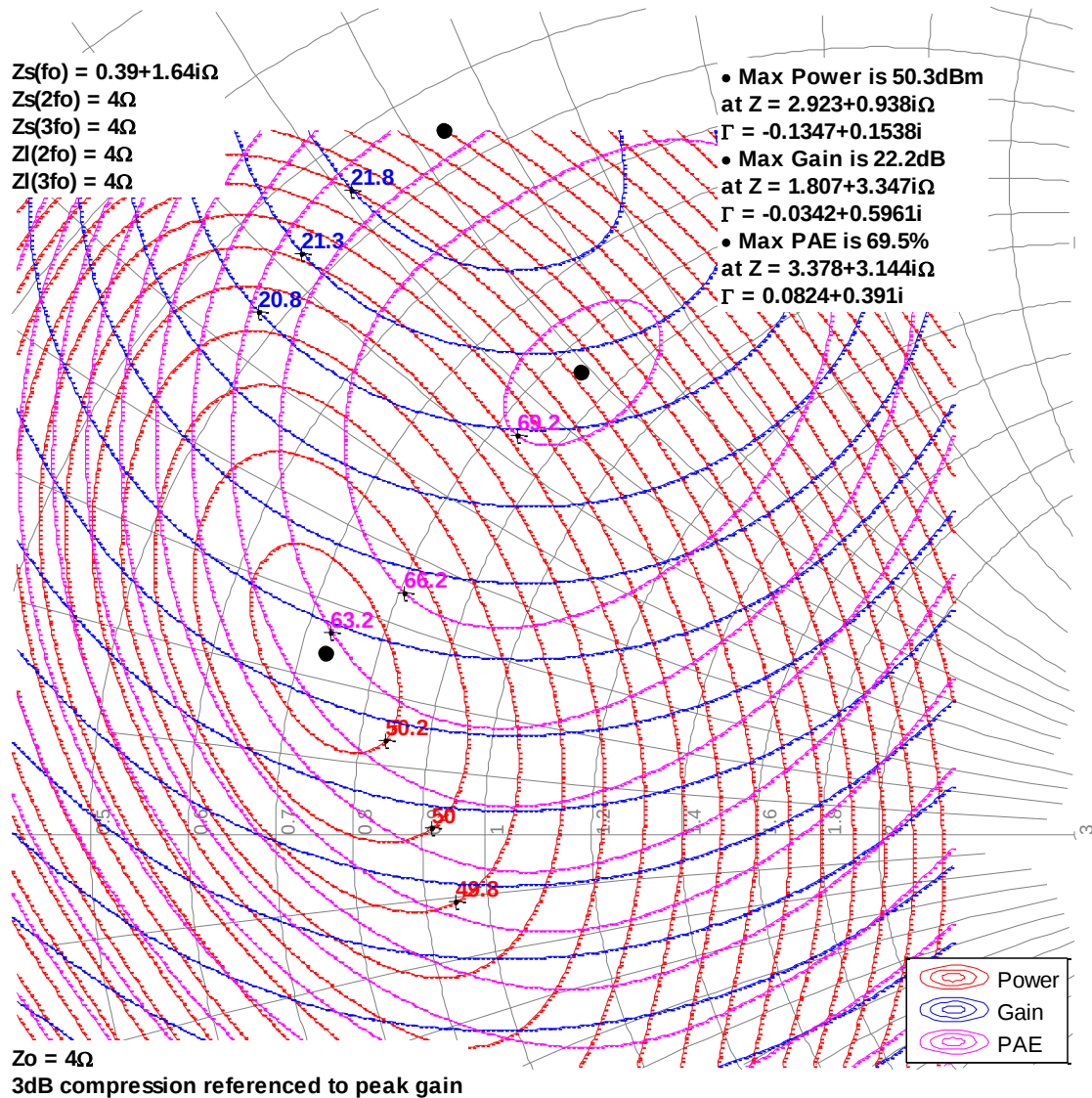
Model Maximum Gain Performance



Model Load Pull Contours

Test Conditions: $V_D = +28\text{ V}$, $I_{DQ} = 400\text{ mA}$, $T = +25^\circ\text{C}$, Pulse (10% Duty Cycle, 100 μs Width).

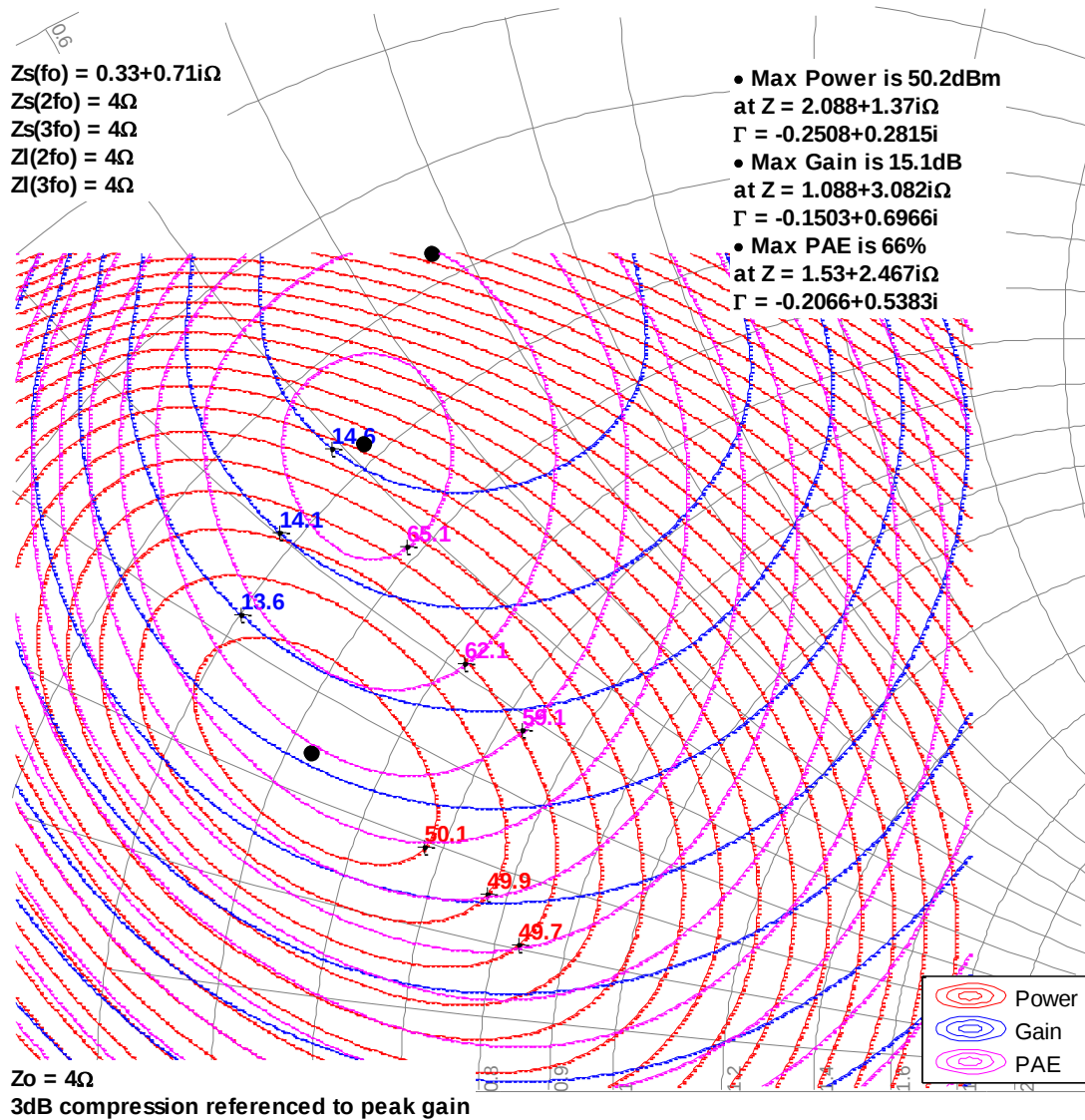
3GHz, Load-pull



Model Load Pull Contours

Test Conditions: $V_D = +28$ V, $I_{DQ} = 400$ mA, $T = +25^\circ\text{C}$, Pulse (10% Duty Cycle, 100 μs Width).

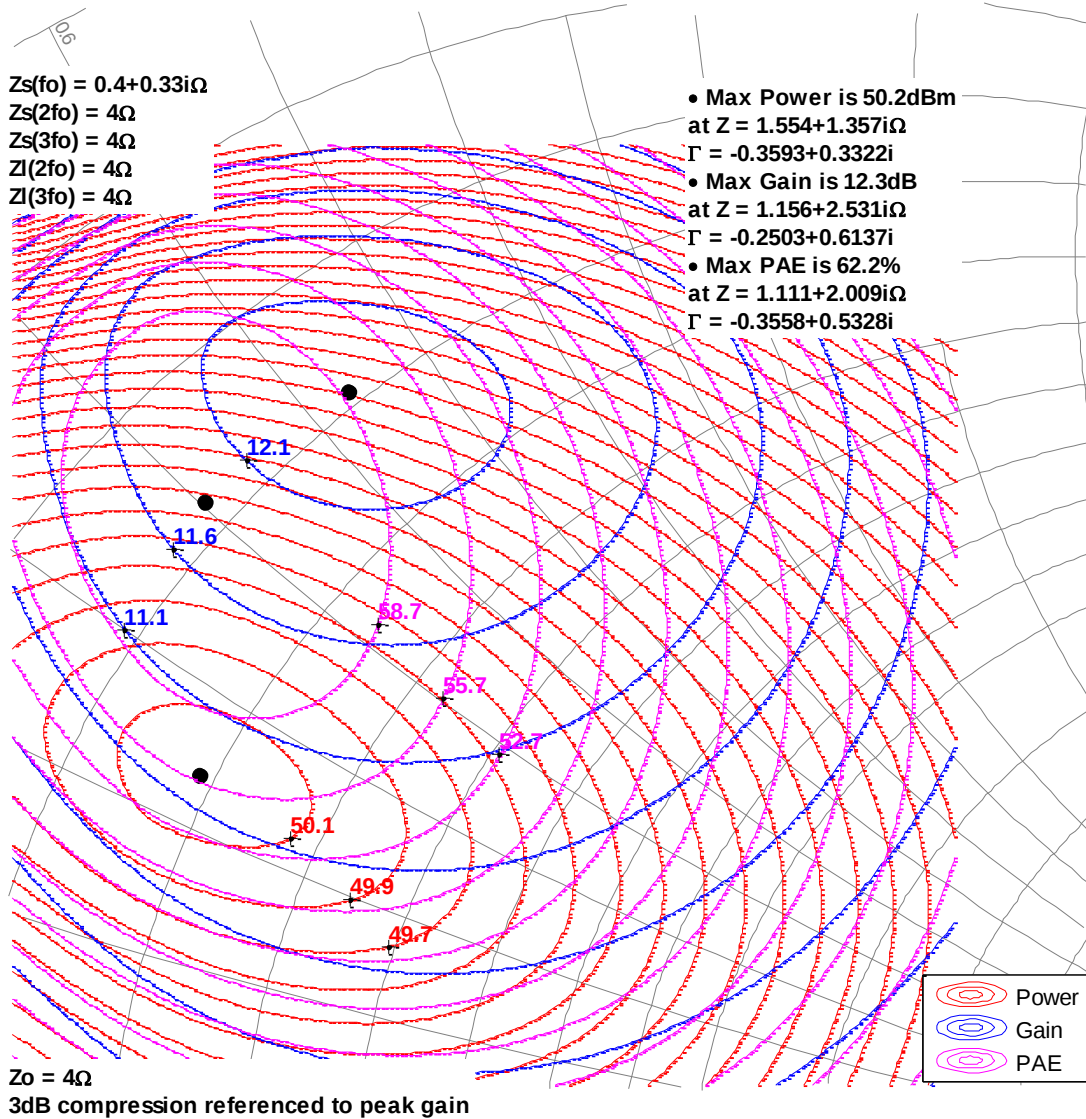
6GHz, Load-pull



Model Load Pull Contours

Test Conditions: $V_D = +28$ V, $I_{DQ} = 400$ mA, $T = +25^\circ\text{C}$, Pulse (10% Duty Cycle, 100 μs Width).

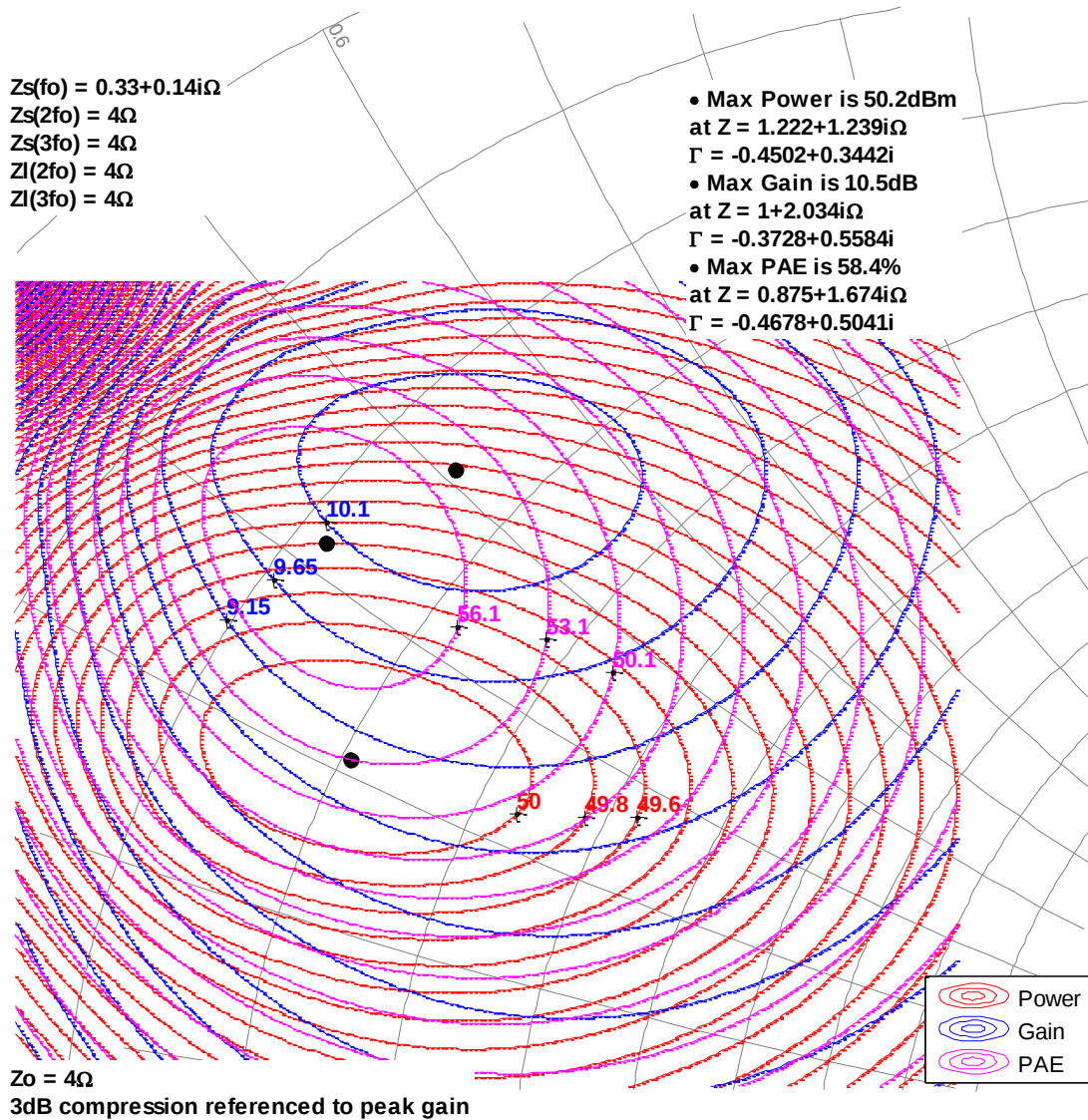
8GHz, Load-pull



Model Load Pull Contours

Test Conditions: $V_D = +28$ V, $I_{DQ} = 400$ mA, $T = +25^\circ\text{C}$, Pulse (10% Duty Cycle, 100 μs Width).

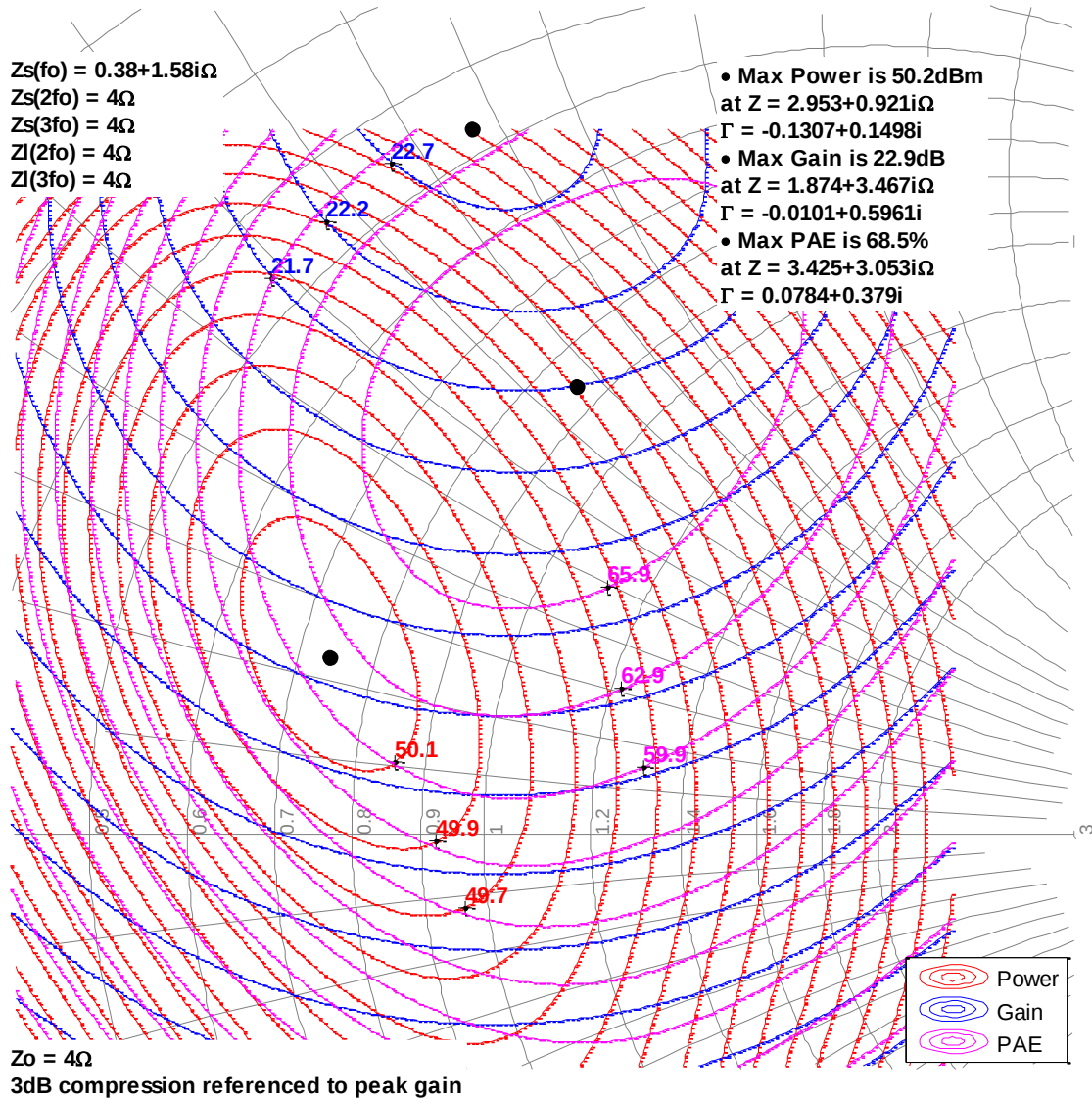
10GHz, Load-pull



Model Load Pull Contours

Test Conditions: $V_D = +28$ V, $I_{DQ} = 1000$ mA, $T = +25^\circ\text{C}$, Pulse (10% Duty Cycle, 100 μs Width).

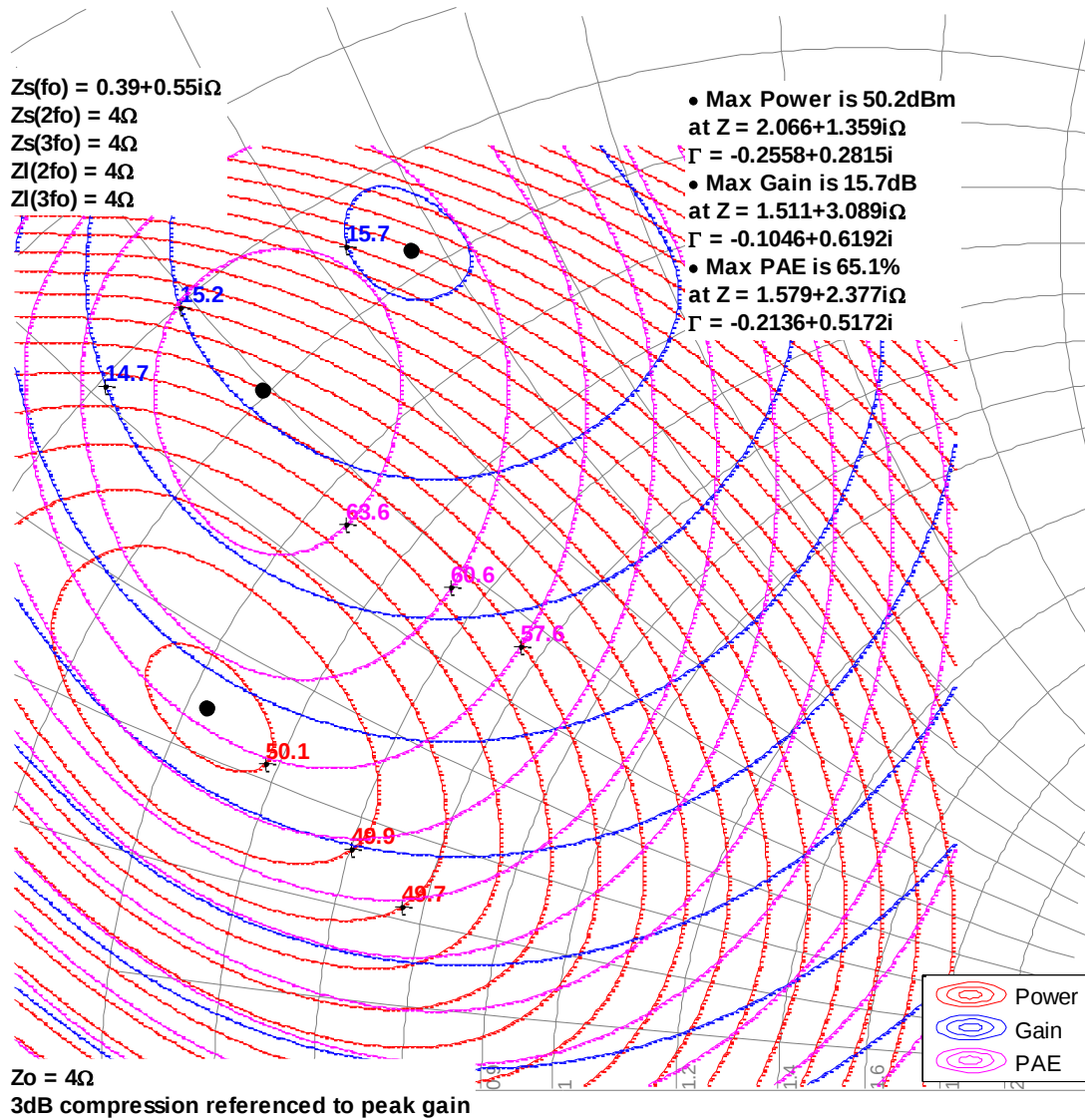
3GHz, Load-pull



Model Load Pull Contours

Test Conditions: $V_D = +28$ V, $I_{DQ} = 1000$ mA, $T = +25^\circ\text{C}$, Pulse (10% Duty Cycle, 100 μs Width).

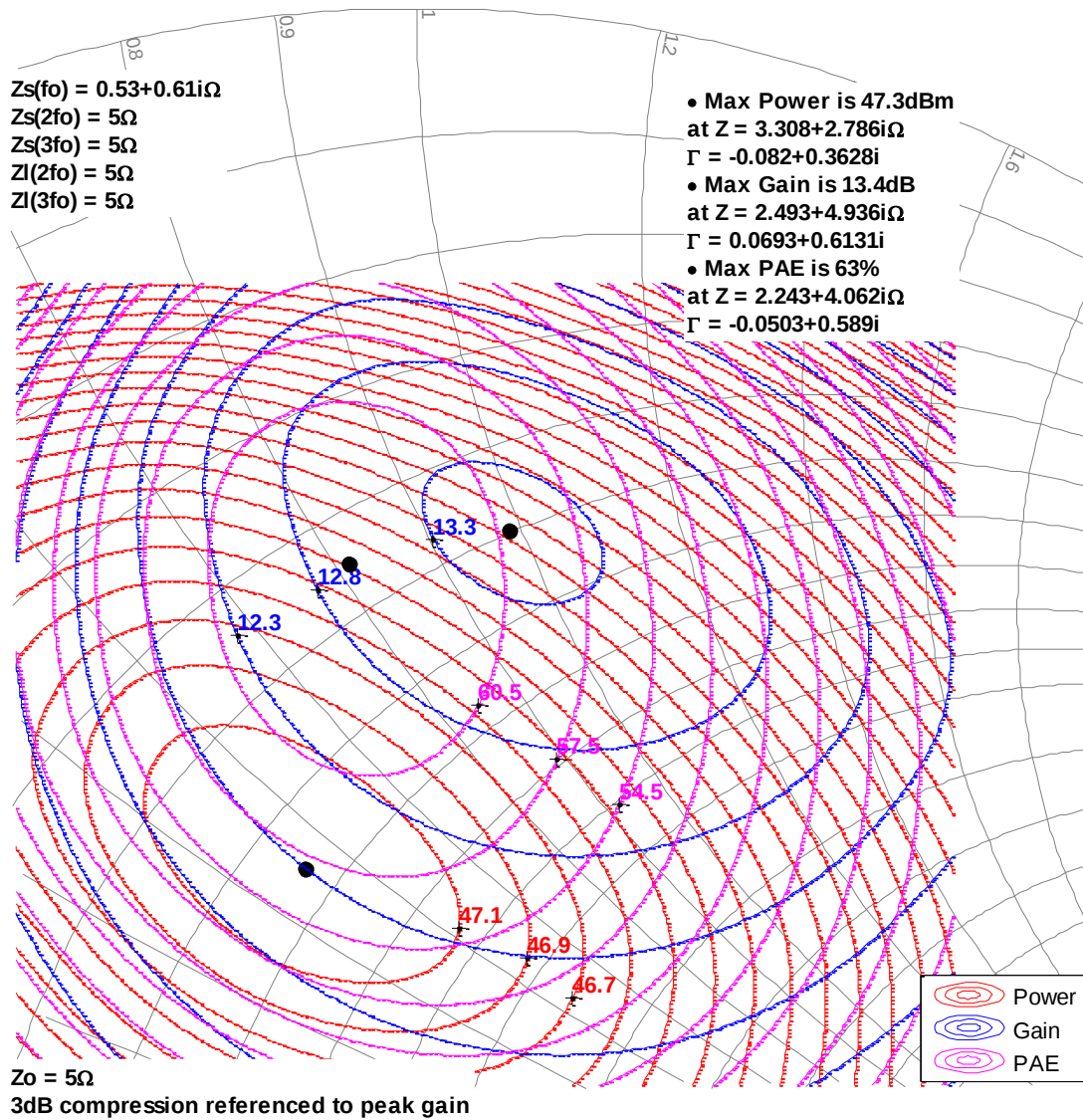
6GHz, Load-pull



Model Load Pull Contours

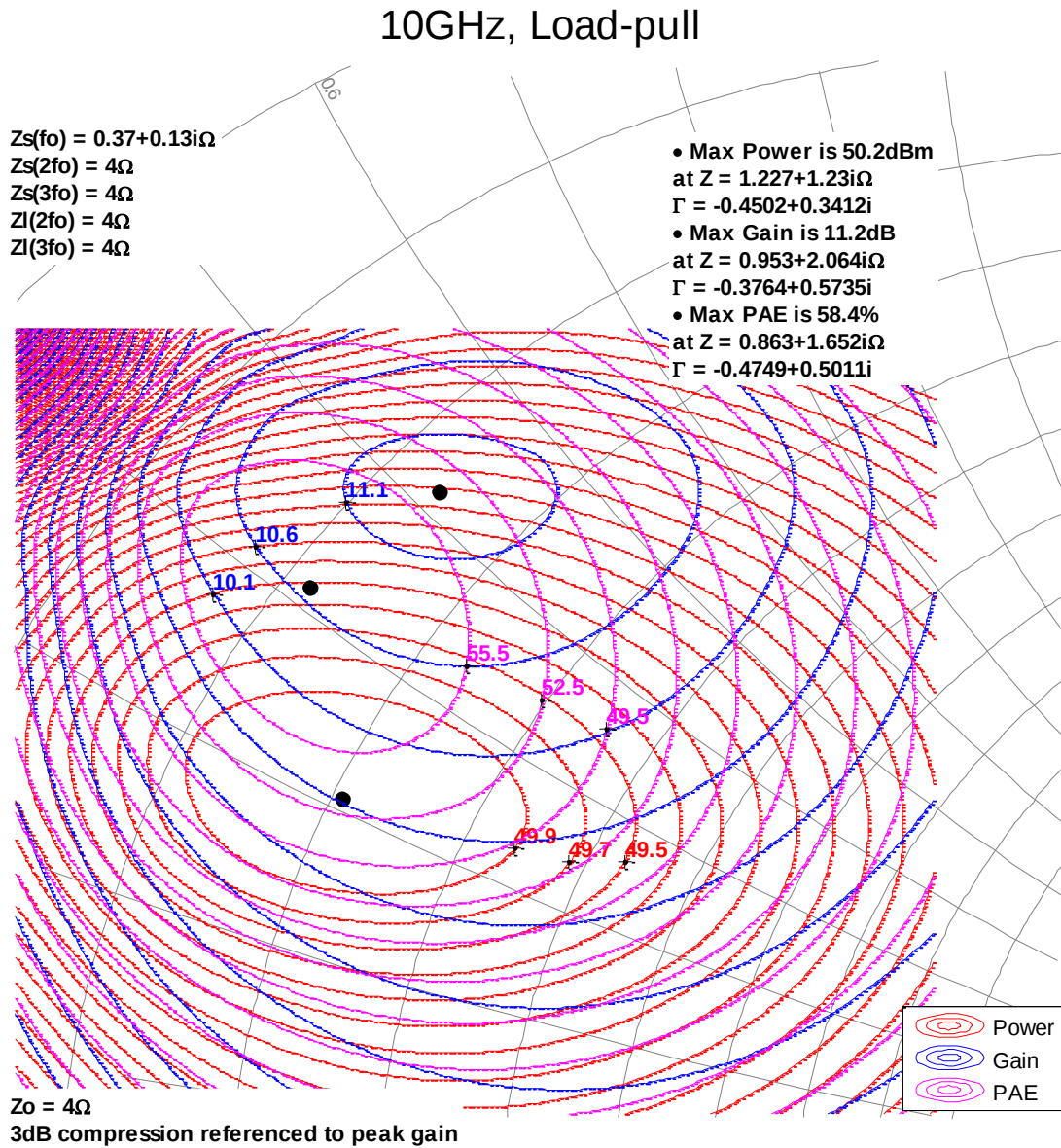
Test Conditions: $V_D = +28$ V, $I_{DQ} = 1000$ mA, $T = +25^\circ\text{C}$, Pulse (10% Duty Cycle, 100 μs Width).

8GHz, Load-pull

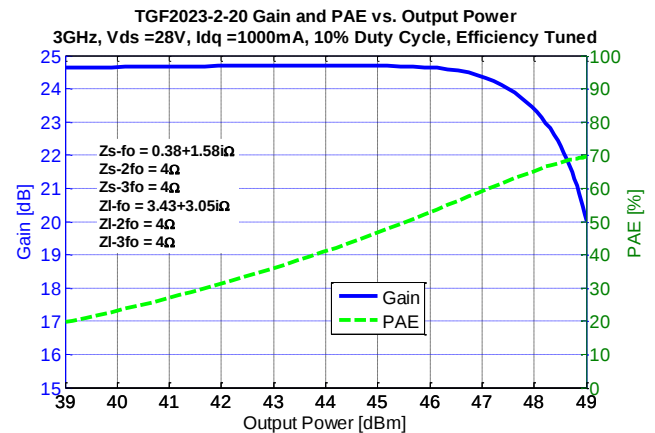
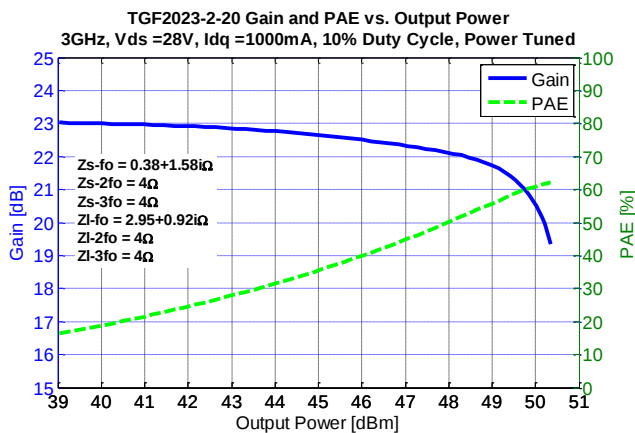
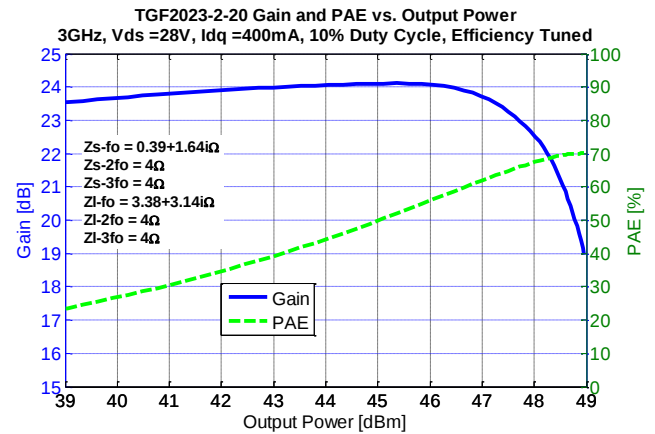
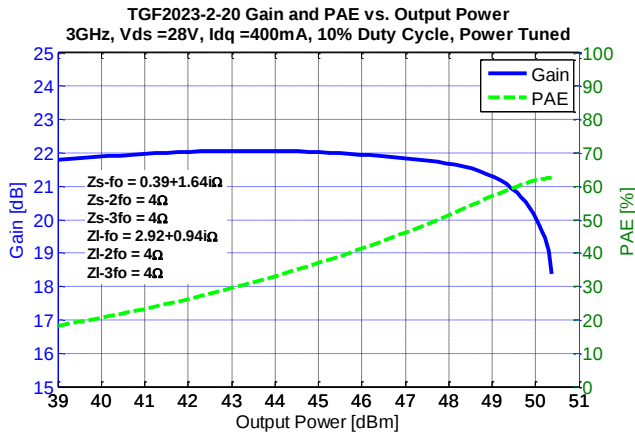


Model Load Pull Contours

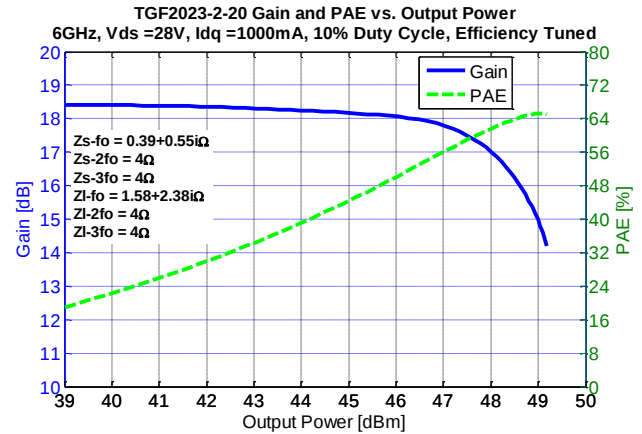
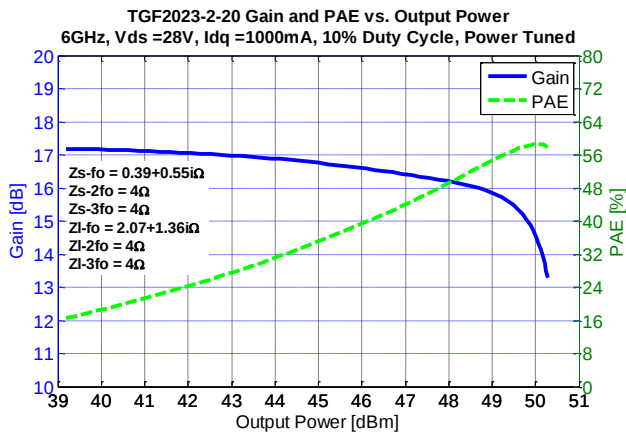
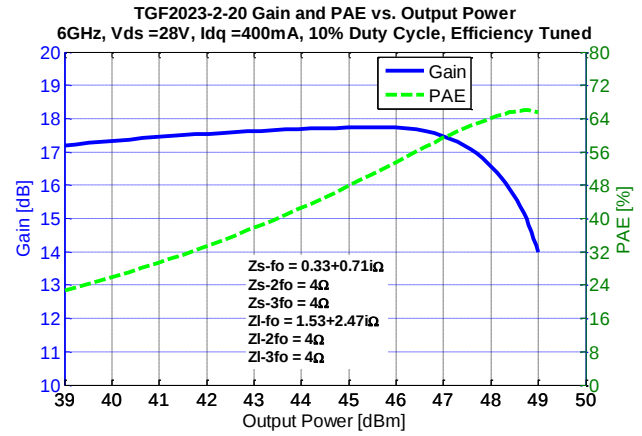
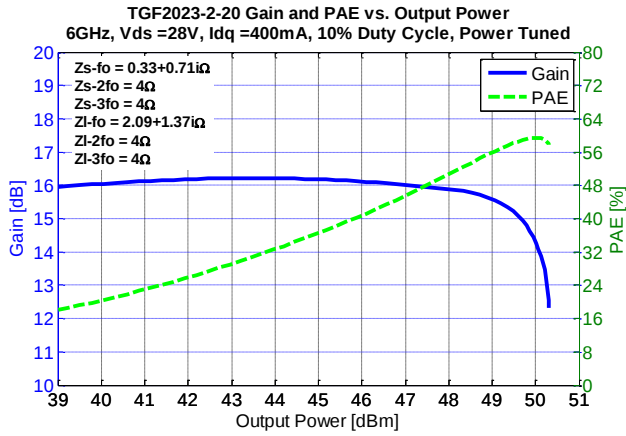
Test Conditions: $V_D = +28$ V, $I_{DQ} = 1000$ mA, $T = +25^\circ\text{C}$, Pulse (10% Duty Cycle, 100 μs Width).



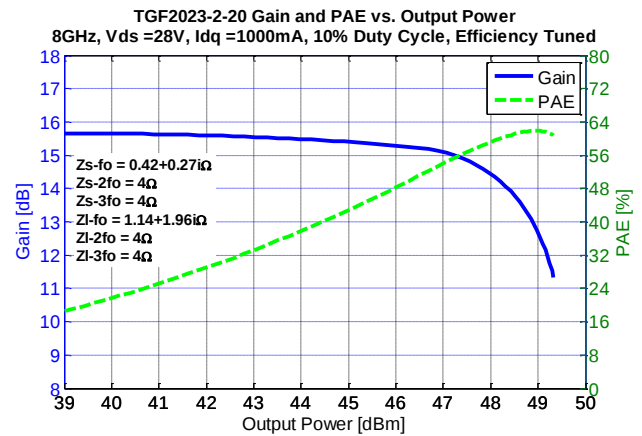
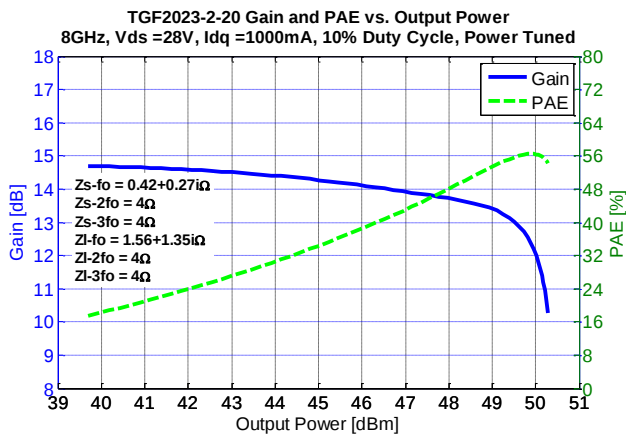
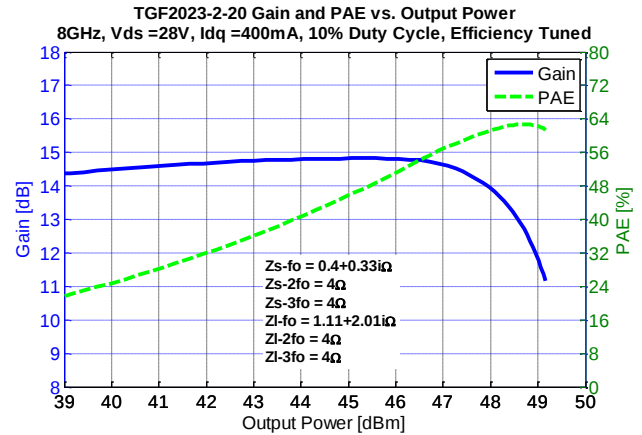
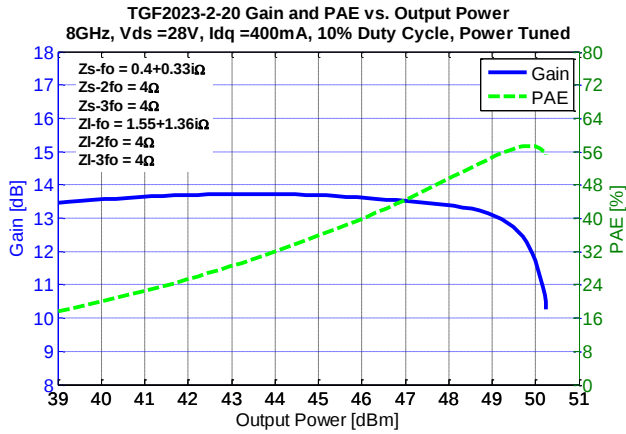
Model Drive-Up Data – 3 GHz



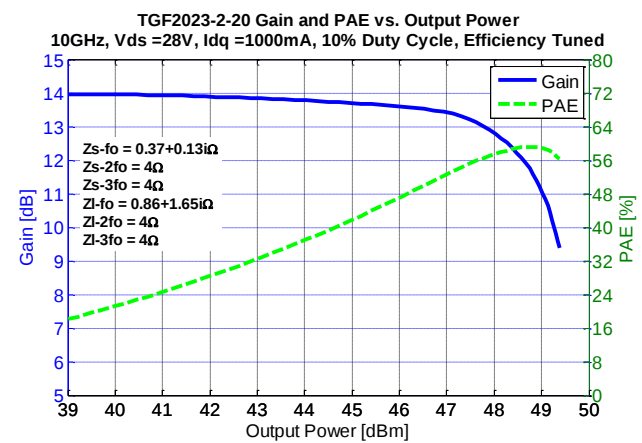
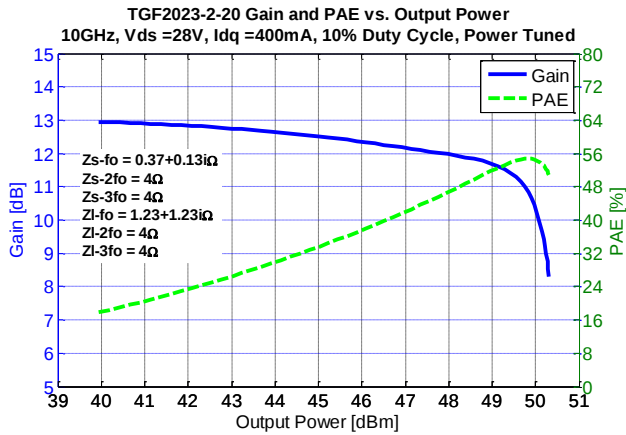
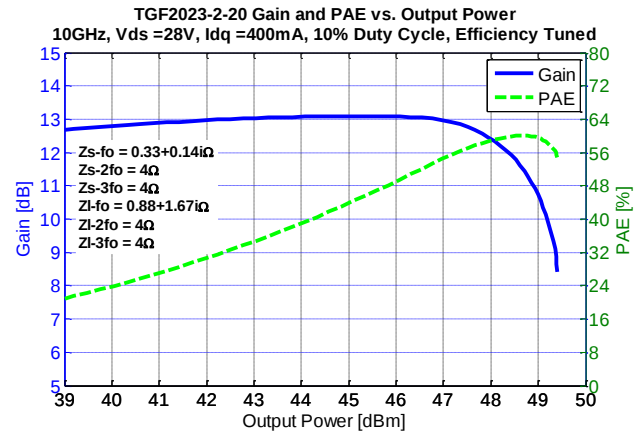
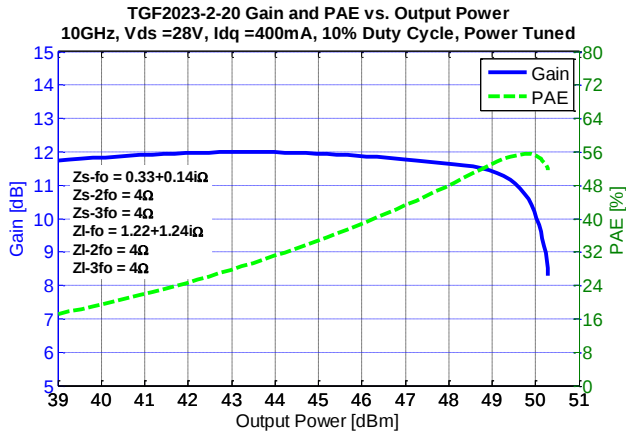
Model Drive-Up Data – 6 GHz



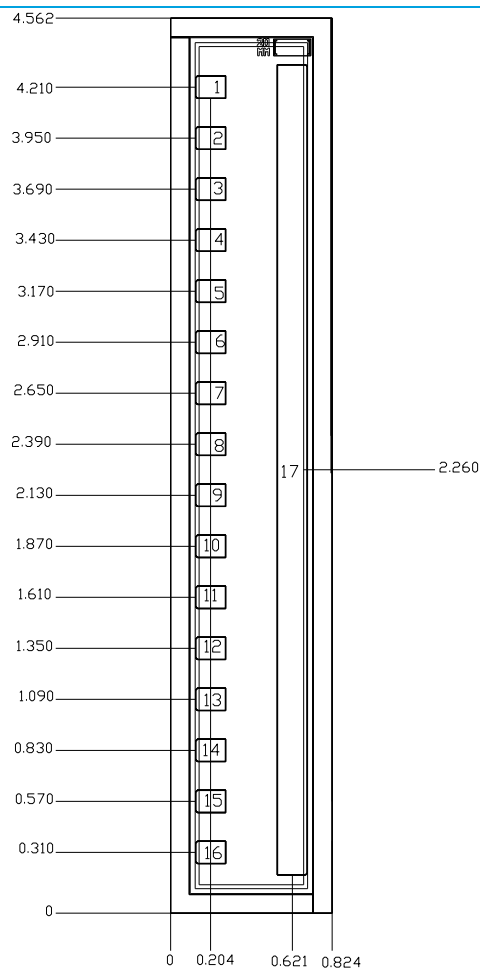
Model Drive-Up Data – 8 GHz



Model Drive-Up Data – 10 GHz



Mechanical Drawing



Bond Pads

Pad No.	Description	Dimensions
1-16	Gate	0.154 x 0.115
2	Drain	0.154 x 4.130
Die Backside	Source / Ground	0.824 x 4.562

1. Units: millimeters
2. Thickness: 0.100 mm
3. Die xy size tolerance: ± 0.050 mm

Model

A model is available for download from Modelithics (at <http://www.modelithics.com/mvp/Qorvo&tab=3>) by approved Qorvo customers. The model is compatible with the industry's most popular design software including Agilent ADS and National Instruments/AWR applications. Once on the Modelithics web page, the user will need to register for a free license before being granted the download.

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e. epoxy) not recommended.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300°C to 3-4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Ball bonding is the preferred interconnect technique, except where noted on the assembly diagram.
- Force, time, and ultrasonics are critical bonding parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Disclaimer

GaN/SiC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Bias Procedure

Bias-Up Procedure

1. Set V_G to -5 V.
2. Set I_D limit to 1100 mA.
3. Apply +28 V to V_D .
4. Slowly adjust V_G until I_D is set to 1000 mA.
5. Set I_D limit to 8 A.
6. Apply RF.

Bias-Down Procedure

1. Turn off RF signal.
2. Turn off V_D .
3. Wait two (2) seconds to allow drain capacitor to discharge.
4. Turn off V_G .

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B (500 V)	ANSI/ESDA/JEDEC Standard JS-001
ESD – Charged Device Model (CDM)	N/A	ANSI/ESDA/JEDEC Standard JS-002
MSL – Moisture Sensitivity Level	N/A	IPC/JEDEC Standard J-STD-020

Not HAST compliant.



Solderability

Compatible with gold/tin (320°C maximum reflow temperature) soldering processes.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

Important Notice

The information contained herein is believed to be reliable; however, Qorvo makes no warranties regarding the information contained herein and assumes no responsibility or liability whatsoever for the use of the information contained herein. All information contained herein is subject to change without notice. Customers should obtain and verify the latest relevant information before placing orders for Qorvo products. The information contained herein or any use of such information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights, whether with regard to such information itself or anything described by such information. **THIS INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.**

Without limiting the generality of the foregoing, Qorvo products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death.

Copyright 2019 © Qorvo, Inc. | Qorvo is a registered trademark of Qorvo, Inc.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Qorvo:](#)

[TGF2023-2-20](#)